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09/527,343	03/17/2000	Timothy E. Giorgetta	AMCC4100	3311

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EXAMINER	
WILSON, ROBERT W	

ART UNIT	PAPER NUMBER
2661	7

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/527,343	GIORGETTA ET AL.	
	Examiner	Art Unit	
	Robert W Wilson	2661	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 November 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1.0 The application of Timothy E. Giorgetta et al. for "Transposable Frame Synchronization Structure" filed 3/17/2000 without a foreign priority has been examined. Claims 1-31 are pending.

Claim Rejections - 35 USC § 102

2.0 The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

3.0 Claims 1-15 are rejected under 35 U.S.C. 102(e) as being anticipated by Sorgi (U.S. Patent No.; 6,493,847)

Referring to **Claim 1**, Sorgi (U.S. Patent No.: 6,493,847) teaches: A method for varying the frame synchronization structure of an information stream (The synchronization frame structure is varied in SONET Frames upon multiplexing 12 STS-1s into one STS-12 per Fig 3A, Fig 2A, and Fig 2B respectively. Please note that there are 12 A1 bytes present in the STS-12 per Fig 2B. Each of the A1 bytes corresponds to the STS-1 which has been multiplexed into the STS-12)

Selecting a first arrangement of synchronization bits in the first stream (The A1 bytes of each STS-1 are selected in order to create STS-3 and the A1 bytes of the STS-3 are selected to create the A1 bytes of the STS-12 per Fig 3A, Fig 2A, and Fig 2B respectively)

In response to selecting the first arrangement of synchronization bits, synchronizing the first stream of information in the first frame structure (The A1 bytes in the STS-1 are selected into the STS-3 and the A1 bytes of the STS-3s are selected in order to build the synchronization bites of STS-12 or SONET frame structure per Fig 3A, Fig 2A, and Fig 2B respectively)

In Addition:

Regarding **Claim 2**, synchronization of the first stream of information includes: reading the first arrangement of the synchronization bits in the first stream of information (The muxes shown in Fig 3A read the A1 bits in the SONET frames shown in Fig 2A in order to create the frame shown in Fig 2B)
In response to reading the first arrangement of synchronization bits, organizing the first information stream into header and data sections (The A1s are organized into the SONET frame of Fig 2B)

Regarding **Claim 3**, in which the selection of the first arrangement of synchronization bits includes selecting the first arrangement of the bits in the header section (The SONET MUXes per Fig 3A select the A1 bytes in the header section as shown in Figs 2A and 3B respectively)

Regarding **Claim 4**, in which the organization of the first stream of information into the first frame structure of header and data sections includes each header section having a plurality of M bits (The header structure of the STS-1 frame shown in Fig 2A has consists of a plurality of M bits)

In which the selection of the first arrangement of synchronization bits includes a selecting a number of bits in the range from zero to M bits in the header (The applicant broadly claims "selecting a number of bits in the range from zero to M bits in the header" The examiner interprets selection of the A1 bytes associated with each SONET frame in the header as "selecting a number of bits in the range from zero to M bits in the header" as shown per Fig 3A, Fig 2A, and Fig 2B.)

Regarding **Claim 5**, in which the selection of the first arrangement of synchronization bits includes selecting the bit position of each synchronization bit in the header (Upon multiplexing STS-1s into a STS-12 the muxes select the bit position of each A1 byte in the header per Fig 3A, Fig 2A, and Fig 2B.)

Regarding **Claim 6**, in which the selecting of the first arrangement of synchronization bits includes selecting the content of the bits in the selected bit positions in the header (The content of the A1 bytes are selected when multiplexing STS-1 into a STS-12 per Fig 3A, Fig 2A, and Fig 2B.)

Regarding **Claim 7**, further deinterleaving the first stream of information into a plurality of n parallel data stream; in which the organization of the first stream of information into the first frame structure includes each parallel data stream having a header and a data section (Deinterleaving the STS-3 per Fig 3A, Fig 2A, and Fig 2B shows parallel data streams of Transport overhead bytes each associated with an STS-1.) in which the selection of the first arrangement of synchronization bits includes selecting n arrangements of synchronization bits, one arrangement for each parallel data stream header section (In creating a STS-12, n=12 arrangements of parallel byte streams are selected per Fig 3A, Fig 2A, and Fig 2B.)

Regarding **Claim 8**, in which the selection of the first arrangement of synchronization bits in the header sections of the n parallel data streams includes selecting a unique arrangement of synchronization for each parallel data stream header section (The applicant broadly claims "unique arrangement of synchronization for each parallel data stream header section" The muxes select the arrangement of synchronization for each of parallel data streams in the header section per Fig 3A, Fig 2A, and Fig 2B)

Regarding **Claim 9**, in which the deinterleaving of the first stream of information includes forming four parallel data streams (Deinterleaving the STS-1 includes forming four parallel data stream ie, headed by A1, A2, J0, & J1 per Fig 2A) in which the reading of synchronization bits from the header sections of the parallel data streams includes reading a first group of the synchronization bits from the first parallel data stream header section (A1 parallel stream per Fig 2A), a second group of synchronization bits from the second parallel data stream header (A2 parallel stream per Fig 2A), a third group of synchronization bits from the third parallel data stream header section (J0 parallel stream per Fig 2A), and a fourth group of synchronization bits from the fourth parallel data stream header section (J1 parallel stream per Fig 2A)

Regarding **Claim 10**, in which the selection of the first arrangement of overhead bits includes: selecting a bit position for each of the first group of bits in the first header section (The mux selects the bit position of the A1 group as shown in Figs 3A, Fig 2A, and Fig 2B respectively) Selecting a bit position for each of the second group of bits in the second header section (The mux selects the bit position of the A2 group as shown in Figs 3A, Fig 2A, and Fig 2B respectively) selecting a bit position for each of the third group of bits in the third header section (The mux selects the bit position of the J0 group as shown in Figs 3A, Fig 2A, and Fig 2B respectively)
Selecting a bit position for each of the fourth group of bits in the fourth header section (The mux selects the bit position of the J1 group as shown in Figs 3A, Fig 2A, and Fig 2B respectively)

Regarding **Claim 11**, in which the selection of the first arrangement of synchronization bits includes selecting the number of synchronization bits in the first, second, third and fourth groups of synchronization (The SONET mux selection the A1, A2, J0, and J1 groups from the STS-1 header per Figs 3A, Fig 2A, and Fig 2B)

Regarding **Claim 12**, organizing a second stream of information in the first frame structure (A2 group per Figs 3A, Fig 2A, and Fig 2B) selecting a second arrangement of synchronization bits to be written in the header section of the second stream of information(A2 group is written per Figs 3A, Fig 2A, and Fig 2B)

Regarding **Claim 13**, further comprising transmitting the second stream of information with the second arrangement of synchronization bits (The muxes transmit the STS data with the A2 group of synchronization bits per Figs 3A, Fig 2A, and Fig 2B)

Regarding **Claim 14**, in which the second stream of information is organized into a plurality of n parallel data streams (The STS-12 is organized into a plurality of N parallel data streams per Figs 2A and 2B), in which the selection of the second arrangement of synchronization bits includes writing n arrangements of synchronization bits (The STS-12 has n synchronization bits per Fig 2B), one arrangement for each parallel data stream header section (The bits are all in parallel per Fig 2B ; and further interleaving the n parallel data streams in to the second stream of information (The 4 parallel header streams from each STS-1 are interleaved into the STS-12 per Fig 2B)

Regarding **Claim 15**, in which the reception of the first stream of information includes receiving the information in a protocol selected from the groups consisting of datacom, telecom, fiber channel, SONET, SDH, and Gigbit Ethernet protocols (SONET and SDH per Abstract)

Claim Rejections - 35 USC § 103

5.0 The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6.0 Claims 19-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sorgi (U.S. Patent No.; 6,493, 847).

Referring to **Claim 19**, Sorgi (U.S. Patent No.; 6,493, 847) teaches: A selectable frame synchronization structure in a transmission frame repeater (The synchronization frame structure is varied in SONET Frames by the muliplexer or transmission frame repeater which multiplexing 12 STS-1s into one STS-12 per Fig 3A, Fig 2A, and Fig 2B respectively. Please note that there are 12 A1 bytes present in the STS-12 per Fig 2B. Each of the A1 bytes corresponds to the STS-1 which has been multiplexed into the STS-12)

A repeater input port to accept a first stream of information including a first arrangement of synchronization bits (Multiplexer shown in Fig 3A has a input port or repeater input port which accepts the STS-1 Streams per Fig 2A which includes A1 bytes or a first arrangement of synchronization bits per Fig 2A)

A decoder having a first input connected to the repeater input port to receive the first stream information, the decoder reading the first arrangement of synchronization bits to organize the first stream of information into a first frame structure including a data section and a header section (The mux or decoder reads A1 byte in the STS-1 frame in order to create the STS-12 frame per Figs 3A, 2A, and 2B)

A decoder having a first input connected to the repeater input port to receive the first stream of information, the decoder reading the first arrangement of synchronization bits to organize the first stream of information, the decoder having a second input for selecting the first arrangement of the synchronization bits to be read (The multiplexer is connected to the input port for receiving the first stream of information per Fig 3A. the multiplexer or decoder reads the A1 bytes associated with the STS-1. The multiplexer selects the A1 bytes associated with each of the STS-1s per Fig 2A and inserts them into the STS-12 frame per Fig 2B).

In Addition:

Regarding **Claim 20** in which the decoder synchronizes the first stream of information into the first frame structure including a header section having a plurality of m bits (STS-1 frame per Fig 2A)
In which the decoder selection of the first arrangement of the overhead bits include selecting a number of synchronization bits in the range from zero to m bits (The A1 bytes of STS-1 are overhead bits which are selecting for creating the STS-12 frame and they range from zero to m bits per Figs 3A, 2A, and 2B)

Regarding **Claim 21**, in which the decoder selection of the first arrangement of synchronization bits includes selecting the bit position of the synchronization bits in the header section (The multiplexer or decoder selects the A1 bytes from the STS-1 frame in bit same bit position in the header for the STS-1 as in the STS-12 per Fig 2A and Fig 2B)

Regarding **Claim 22**, in which the decoder selection of the first arrangement of synchronization bits includes selecting the content of each synchronization bit in the header section (The multiplexer or decoder selects the content of the A1 bytes associated with the STS-1 frame when building the STS-12 frame)

Regarding **Claim 23**, further comprising: a deinterleaver circuit having an input to receive the first stream of information the deinterleaver circuit deinterleaving the first stream of information into a plurality of n parallel data streams (The multiplexer performs the function of breaking the STS-1 header into parallel data streams in order to build an STS-13 per Figs 2A and 2B)

In which the decoder's first input includes a plurality of n inputs connected to the deinterleavers to receive the first stream of information in n parallel data streams (The STS-1 consists of n parallel streams of information per Fig 2A) the decoders's selection of the first arrangement of synchronization bits includes selecting an arrangement of synchronization bits each of the n parallel data streams to form a first frame structure including header and data sections in each data stream (The multiplexer selects parallel data streams of header information from the STS-1s in order to build the STS-12 per Figs 2A and 2B)

Regarding **Claim 24**, in which the decoder's selection of the first arrangement of overhead bits includes selecting independent arrangements of synchronization bits for each header section of the n parallel data streams (The multiplexer selects independent and parallel bit streams from the STS-1 in order to build an STS-12 per Figs 2A and 2B)

Regarding **Claim 25**, in which the deinterleaver circuit de interleaves the first stream of information into four data streams (The multiplexer deinterleaves the STS-1 into a A1, A2, J0, and J1 data stream in order to build an STS-12 per Figs 2A and 2B)

In which the decoder's selection of the first arrangement of synchronization bits includes reading a first group of bits from the first parallel data stream header section (Reads A1 stream in order to build an STS-12 from 12 STS-1s per Figs 2A and 2B)

Reading a second group of bits from the second parallel data stream header (Reads A2 stream in order to build an STS-12 from 12 STS-1s per Figs 2A and 2B)
Reading a third group of bits from the parallel data stream header section (Reads J0 stream in order to build an STS-12 from 12 STS-1s per Figs 2A and 2B)
Reading a fourth group of bits from the fourth parallel data stream header section (Reads J1 stream in order to build an STS-12 from 12 STS-1s per Figs 2A and 2B)

Regarding **Claim 26**, further comprising an encoder having an output to provide the second stream of information organized in the first frame structure with header sections

The encoder having an input for selecting a second arrangement of synchronization bits to be written in the header section (The multiplexer selects the A2 stream from each STS-1 when building a STS-12 per Figs 2A and 2B)
A repeater output connected to the encoder output to provide the second stream of information (The mux output provides the second stream of information per Fig 2A and 2B)

Regarding **Claim 27**, in which the encoder organizes the second stream of information into a plurality of n parallel data streams (The mux organizes the STS-12 into n parallel streams per Fig 2B) and in which the encoder selection of the second arrangement of synchronization bits includes selecting the synchronization bits to be written in the header sections of n parallel data streams (The mux selects the N parallel streams of synchronization bits in builds them into the frame of Fig 2B) and further comprising: an interleaver circuit having a plurality of n inputs connected to n encoder outputs, the interleaver circuit interleaving the parallel data streams in to

a second stream of information, the interleaver circuit having an output connected to the repeater output (Fig 2B)

Regarding **Claim 28** in which the repeater input receives the first stream of information in a protocol selected from the group consisting of datacom, telecom, fiber channel, SONET, SDH, and Gigbit Ethernet protocols (SONET and SDH per Abstract

Sorgi does not expressly call for: a second input on the decoder but teaches the multiplexer which performs the functions shown in Figs 3A, 2A, and 2B.

It is within the level of one skilled in the art to implement the functions of Sorgi in hardware and software. The function of selecting the A1 bytes from the STS-1 when building the STS-3 are defined in Figs 3A, 2A, and 2B consequently it would have been obvious to one of ordinary skill in the art at the time of the invention implement a second input on the decoder to select the A1 bytes when multiplexing STS-1s into a STS-12.

Referring to **Claim 29**, Sorgi (U.S. Patent No.; 6,493, 847) teaches: A selectable frame synchronization structure communications system (Fig 1 or system . The synchronization frame structure is varied in SONET Frames by the muliplexer or transmission frame repeater which multiplexing 12 STS-1s into one STS-12 per Fig 3A, Fig 2A, and Fig 2B respectively. Please note that there are 12 A1 bytes present in the STS-12 per Fig 2B. Each of the A1 bytes corresponds to the STS-1 which has been multiplexed into the STS-12)

A transmitter having an output to provide the first stream of information in the first frame structure with a header including a first arrangement of synchronization bits (The mux performs the function of outputting the A1 bytes from the STS-1s in order to build the STS-12 per Figs 3A, 2A, and 2B)

A repeater input port to accept a first stream of information including a first arrangement of synchronization bits (The has an input port which accepts the STS-1 A1 bytes per Figs 3A and 2A)

A decoder having a first input connected to the repeater input port to receive the first stream of information, the decoder reading the first arrangement of synchronization bits to organize the first stream of information, the decoder having a second input for selecting the first arrangement of the synchronization bits to be read (The multiplexer is connected to the input port for receiving the first stream of information per Fig 3A. the multiplexer or decoder reads the A1 bytes associated with the STS-1. The multiplexer selects the A1 bytes associated with each of the STS-1s per Fig 2A and inserts them into the STS-12 frame per Fig 2B).

In Addition:

Regarding **Claim 30**, in which the repeater further includes: an encoder having an output to provide a second stream of information organized in the first stream structure with a header section, the encoder having an input for selecting a second arrangement of synchronization bits to be written in the header section (The mux organizes the A2 stream or second stream of data in the STS-1 in order to build the STS-12 header per Figs 2A and 2B) and a repeater output connected to the encoder output to provide the second stream of information (Figs 1 , Fig 2A, Fig 2B , and Fig 3A)

Regarding **Claim 31**, a receiving having an input connected to the repeater output to accept the second stream of information the receiver read the second arrangement of synchronization bits to organize the second stream of information into the first frame structure (Figs 1 , Fig 2A, Fig 2B , and Fig 3A)

Sorgi does not expressly call for: the decoder but teaches the multiplexer which performs the functions shown in Figs 3A, 2A, and 2B.

It is within the level of one skilled in the art to implement the functions of Sorgi in hardware and software. The function of selecting the A1 bytes from the STS-1 when building the STS-3 are defined in Figs 3A, 2A, and 2B consequently it would have been obvious to one of ordinary skill in the art at the time of the invention implement a decoder to select the A1 bytes when multiplexing STS-1s into a STS-12

Response to Amendment

7.0 Applicant's arguments with respect to claims 1-31 have been considered but are moot in view of the new ground(s) of rejection.

The examiner respectively disagrees with the applicant's argument that the reference fails to teach "A method for varying the frame synchronization structure of an information stream;

Selecting a first arrangement of synchronization bits in the first stream;

In response to selecting the first arrangement of synchronization bits, synchronizing the first stream of information in the first frame structure"

Sorgi (U.S. Patent No.: 6,493,847) teaches: A method for varying the frame synchronization structure of an information stream (The synchronization frame structure is varied in SONET Frames upon multiplexing 12 STS-1s into one STS-12 per Fig 3A, Fig 2A, and Fig 2B respectively. Please note that there are 12 A1 bytes present in the STS-12 per Fig 2B. Each of the A1 bytes corresponds to the STS-1 which has been multiplexed into the STS-12)

Selecting a first arrangement of synchronization bits in the first stream (The A1 bytes of each STS-1 are selected in order to create STS-3 and the A1 bytes of the STS-3 are selected to create the A1 bytes of the STS-12 per Fig 3A, Fig 2A, and Fig 2B respectively)

In response to selecting the first arrangement of synchronization bits, synchronizing the first stream of information in the first frame structure (The A1 bytes in the STS-1 are selected into the STS-3 and the A1 bytes of the STS-3s are selected in order to build the synchronization bites of STS-12 or SONET frame structure per Fig 3A, Fig 2A, and Fig 2B respectively)

8.0 Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Conclusion

9.0 Any inquiry concerning this communication or earlier communications from the examiner should be directed to Robert W Wilson whose telephone number is 703/305-4102. The examiner can normally be reached on M-F (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Douglas Olms can be reached on (703) 305-4703. The fax phone numbers for the

organization where this application or proceeding is assigned are (703) 872-9314 for regular communications and (703) 872-9314 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-4700.

Robert W. Wilson

Robert W Wilson
Examiner
Art Unit 2661

RWW
December 11, 2003

RWW
[illegible]